RESEARCH ARTICLE OPEN ACCESS

# Design and Implementation of Digital PLL using Self Correcting DCO System

M.Mohan Babu*, P.Sree Kavya**
* (M.Tech Scholar, Dept. of ECE, SITAMS, Chittoor, AP, India.)
** (Assistant Professor, Dept of ECE, SITAMS, Chittoor, AP, India,)

**ABSTRACT**
The mainstay of the paper is to use a PLL using self healing pre-scalar. When a CMOS technology approaches to a nanometer scale, the non-idealities like variability and leakage current may affect the circuit performances. The process variability leads to the large variations to degrade the device matching and performances. The leakage current is highly dependent upon the process variations. In the existing method the key parameter is to be change the modulus value of the pre- scalar. By changing the value of the pre-scalar the PLL frequency range will be extended. In the proposed design we are planning to implement the digital PLL technique with self correcting DCO. The structure utilizes the DDR synthesizer as a base for generating the DCO frequency, so many methods are there to correct the DCO errors , here we detect the error or delay and correct it by using smooth jumping method. The DPLL varies from minimum system clock frequency 60 to 1489 MHZ (Minimum) maximum of GHZ frequency of any range we can generate, since our design act as a general platform for any kind of application.
**Keywords** - DCO, Delay Detector, Frequency Divider, Self Healing, Signal Shaping Circuit.

## I. INTRODUCTION

Phase locked loops were initially written but not designed. The previous analog design consists of oscillator, a mixer and an audio amplifier. The design was very simple but has drawbacks. Reception after a period of time became difficult due to frequency drift of the local oscillator. Their solution to this problem incorporated a delay detector comparing the input frequency to the reference frequency of the oscillator. The delay detector would output a differential voltage that was fed back into the local oscillator keeping it at the correct frequency. This technique was the same technique that was developed for electronic servo control systems at that time. This was the first iteration in the evolution of the phase locked loop (PLL).

With the development of hardware description languages, digital phase locked loops can be implemented with low cost. The digital techniques are used to reduce area and power consumption and to increase speed of operation.

Phase-locked loops (PLL) have become essential components in wireless communication systems. They are used as frequency synthesizers with precise and convenient digital control in both traditional electronics, such as televisions and AM/FM radios, and modern consumer products among which cellular mobile phone is a striking example.

## II. DESIGN AND IMPLEMENTATION

The proposed digital Phase locked loop is designed as shown in Fig.1 below to eliminate disturbances and leakage currents in analog components.

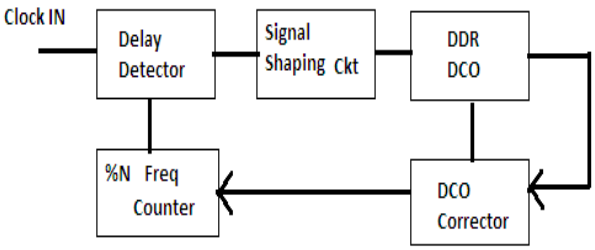


Fig1.Proposed Digital Phase Locked Loop.

In analog implementation, the operation of a classic analog phase locked loop was discussed and as discussed before, operation has the same principle but works not similarly. The parts of the phase locked loop are now present in the digital phase locked loop but they are designed and constructed differently due to the fact that the signals that they deal with are different and CPLD is discrete. The input to the digital PLL is a digital pattern normally from an analog to digital converter or a clock.

In this section, the individual components of the digital phase locked loop will be broken down into their rudimentary components like counters, control bits and memory elements. These are the types of components that can be designed and implemented.

## III. DELAY DETECTOR

The delay detector is implemented as shown in Fig.2 below to determine the delay errors in the feedback loop.

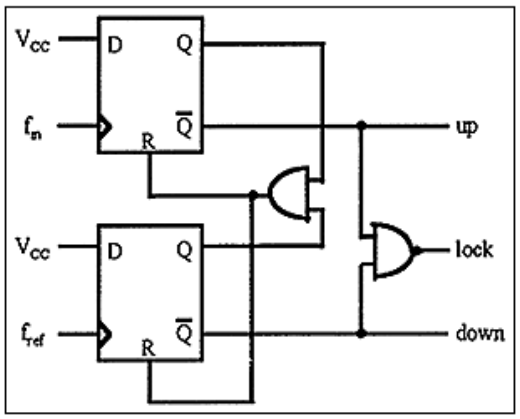


Fig2.Delay Detector

The two inputs of the delay detector are the reference input and the feedback from the DCO. The delay detector output controls the DCO such that the phase difference between the two inputs is held constant, making it a negative feedback system.

## IV. DESIGN OF SIGNAL SHAPING CIRCUIT

The next stage of the loop is the signal shaping circuit. The signal shaping circuit that always works with the EXOR and the edge triggered delay detectors is the mod counter. The mod counter is shown in Fig.3 below.

The block commonly called the for determining its stability. This is how the loop responds to disturbances, such as change in the desired frequency, variation of the frequency counter outputs. Common considerations are the range over which the loop can achieve lock (pull-in range, lock range or capture range), how fast the loop achieves lock (lock time, lock-up time or settling time) and damping behavior. Depending on the application, this may require one or more of the following: a simple proportion (gain or attenuation), an integral (low pass filter) and/or derivative (high pass filter). Loop parameters commonly examined for this are the loop's gain margin and delay margin. Common concepts in control theory including the PID controller are used to design this function.

The signal shaping circuit contains two separate counters both of which are counting in upward or downward manner. The UP/DOWN bit determines which counter is running at any moment. The carry and borrow outputs are the most significant bits of the UP/DOWN counters and are only high when the contents of a particular counter are greater than K/2 where K is modulus value of clock. These values are used to control the digitally controlled oscillator. The counters are reset to initial state when the contents reach a value of K – 1.

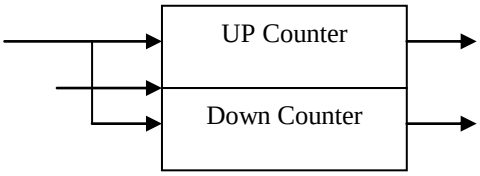


Fig3.Signal Shaping Circuit

## V. Design of DCO & Frequency Divider

5.1. Digital Control Oscillator:

The final part of the digital phase locked loop is the DCO (digitally controlled oscillator) shown in fig4 below. In this DCO is a counter implemented using VHDL coding. A digitally controlled oscillator or DCO is a hybrid digital/analog electronic oscillator used in frequency synthesizers. The name is similar with "voltage-controlled oscillator". DCOs were designed to enhance the tuning stability of applied reference signals.

The delay lock of a Digital Controlled Oscillator for very high frequencies and microwave frequencies is very important in wireless communications and radar application. It combines the delay noise of fundamental oscillators, particularly in the microwave frequency range (100 kHz away from carrier frequency and beyond), the excellent long-term stability, and the close-in delay noise of a crystal oscillator (from carrier frequency to 100 kHz away).A Digital Controlled Oscillator can be delay locked by the following method.

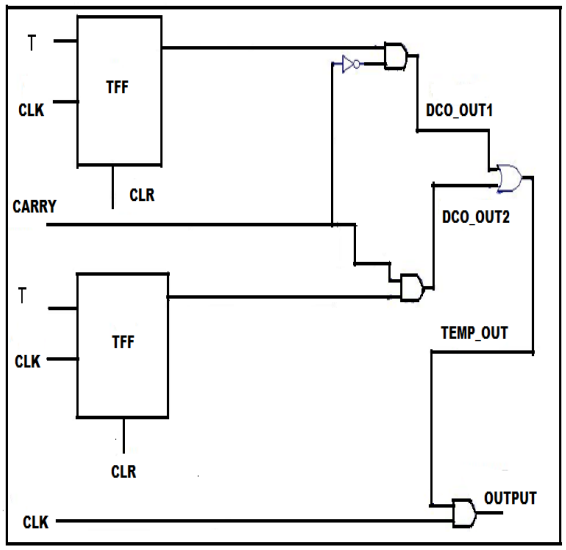


Fig4.Digital controlled Oscillator

5.1.1. Digital delay lock:

This is usually achieved by using a frequency divider to divide the higher frequency of the DCO to the same frequency of the crystal reference. A digital delay detector is then used to acquire the delay lock. The advantage of this method is that it is self-obtaining and can operate at very low frequencies. It is widely used at low frequencies from MHz up to GHz. The two disadvantages of this method are the noise floor of the divider will limit its delay noise and at microwave frequencies it will not be economical.

The DECR and INCR inputs are the carry and borrow outputs from the signal shaping circuit respectively. This part of the loop operates in connection with the frequency counter that works to slow down the clock frequency.

The decrement input to the modified counter causes to take one half-cycle out. Conversely, the increment input causes one half-cycle to be taken out of the output. The adjusted waveform is shown in fig6 below. This variation is constantly maintaining that the cycles stay delay locked.

All of the components implemented above are connected together forming the digital phase locked loop. The digital phase locked loop constantly adjusts the produced wave until it is in delay lock with the input frequency.

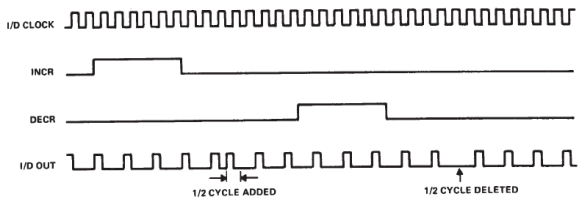


Fig6.Output of DCO

5.2. Frequency Divider:

This is shown in Fig.6 below .Digital PLL's include frequency counter between the reference clock and the reference input to the delay detector to produce a frequency synthesizer. If the frequency counter in the feedback path divides by integer, it allows the PLL to multiply the reference frequency. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be changed by other issues, and then the reference frequency from frequency counter is useful.

Frequency divider is used to generate various reference frequencies applied to the delay detector to compare with the input frequency signal. Frequency multiplication can also be attained by locking the DCO output to the nth harmonic of the reference signal. The DCO output is tuned near to the input frequency.

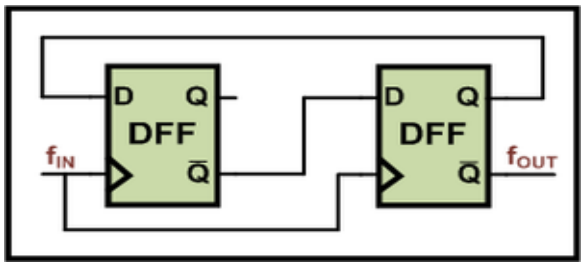


Fig6.Frequency Divider

## VI. EXPERIMENTAL RESULTS AND ANALYSIS

Digital PLL generates output frequency in the range of MHz to GHz. The system consists of five modules .The various outputs for the implementation of digital phase locked loops are shown in below figures.

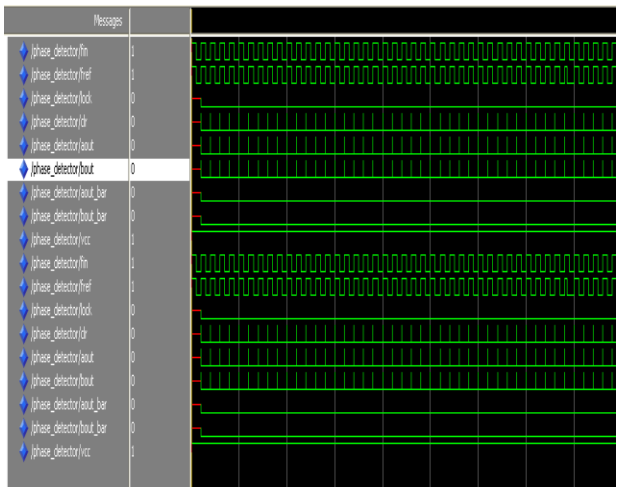


Fig7. Output of Delay Detector

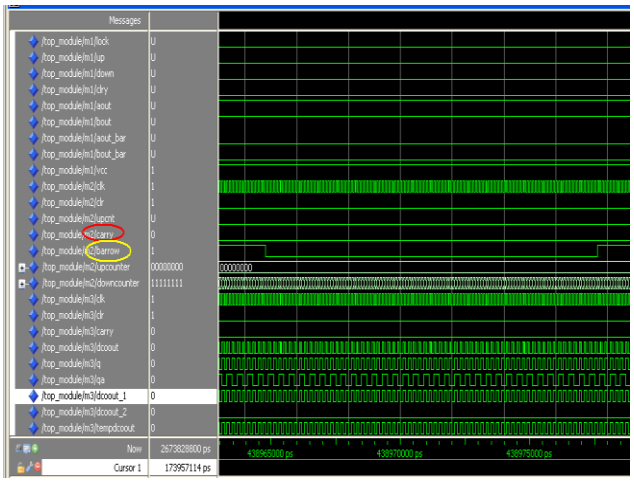


Fig8.Output of Signal Shaping Circuit

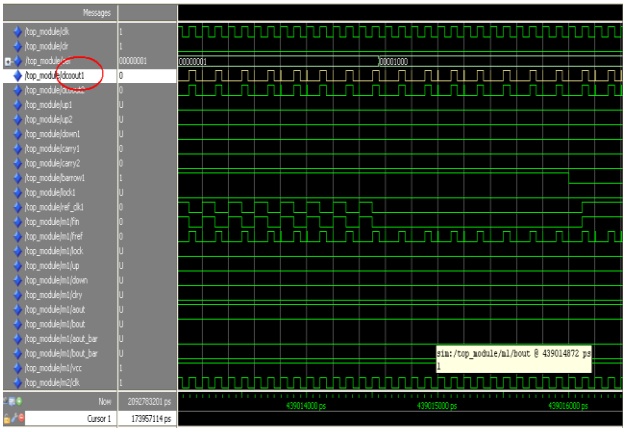

Fig9. Output Of DCO

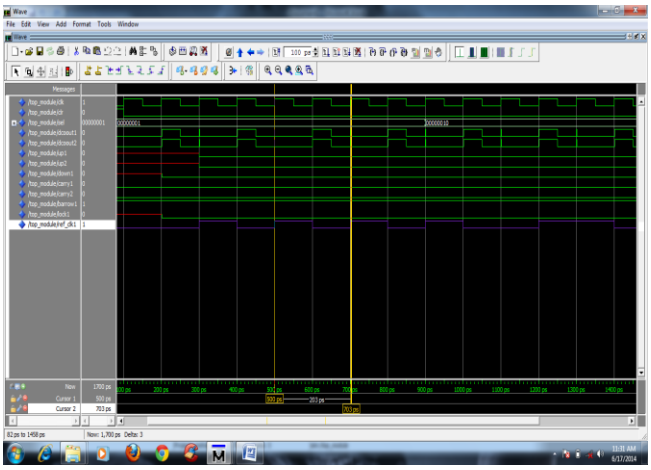

Fig 10. Top Module Output of Digital PLLL

The area used and power supply requirement and delay produced in implementation of the digital phase locked loop is shown in table1 below.

Table1: Xilinx Summary Report

| Area Used | Power Supply | Delay |
|---|---|---|
| 24% | 0.156V | 2.80nSec |

## VII. CONCLUSION AND FUTURESCOPE

6.1. Conclusion:

A digital phase locked loop is designed by integrating delay detector, signal shaping circuit and digital controlled oscillator with frequency counter. It is used in decoders to check the received information is correct or not. If the data bits or clock bits are out of delay then the decoded information could be decoded incorrectly. the input. The loop could also be used to synchronize to a repeatable code. The digital phase locked loop can be used as frequency synthesizer to produce wide range frequencies from MHz to GHz.

6.2. Future Scope:

Further improvement in this paper is to apply phase lock for analog signals by using analog to digital converter. The proposed method uses digital inputs to phase lock in the desired frequency range .By using analog signals, the phase locked loops can be applied to the real time applications like analog communication and wireless communications. The frequency range can be increased by using number of bits used in selection line used in digital controlled oscillator

## REFERENCES

[1] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "*Analog circuit design in nanoscale CMOS technologies*," Proc. IEEE, vol. 18, no. 11, pp. 1687–1714, Oct. 2009.

[2] J. M. Wang, Y. Cao, M. Chen, J. Sun, and A. Mitev, "*Capturing device mismatch in analog and mixed-signal designs*," IEEE Circuits Syst. Mag., vol. 8, no. 4, pp. 137–144, Dec. 2008.

[3] K. Agawa, H. Hara, T. Takayanagi, and T. Kuroda, "*A bitline leakage compensation scheme for low-voltage SRAMs*," IEEE J. Solid-State Circuits, vol. 36, no. 5, pp. 726–734, May 2001.

[4] "*A Digitally Controlled PLL for SoC Applications*" Thomas Olsson, and Peter Nilsson IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 5, MAY 2004 751

[5] "*An All-Digital Phase-Locked Loop with 50-Cycle Lock Time Suitable for High-Performance Microprocessors*" Jim Dunning,, Gerald Garcia, Jim Lundberg, and Ed Nuckolls, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 30, NO. 4, APRIL 1995

[6] "*A fully integrated standard-cell digital PLL*," T. Olsson and P. Nilsson, *IEEElectron. Lett.* vol.37, pp. 211–212, Feb. 2001.

[7] J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "*Digital Integrated Circuits*", 2nd ed.Prentice Hall, 2003, ISBN 0-13-120764-4.

[8] N. Waste and K. Eshraghian, "*Principles of CMOS VLSI Design*", Addison-Wesley, 1993.

## AUTHORS:

1. **Mohan Babu M** is an P.G Scholar in the Department of Electronics & Communication Engineering, in the specialization of VLSI System Design, Sreenivasa Institute of Technology and Management Studies, Chittoor, Andhra Pradesh, India.

2. **Sree Kavya P** is an Assistant professor in the Department of Electronics & Communication Engineering, in the specialization of VLSI System Design, Sreenivasa Institute of Technology and Management Studies, Chittoor, Andhra Pradesh, India.